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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,863	12/02/2003	Haitham H. Akkary	1020.P17876	1592

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EXAMINER	
KROFCHECK, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,863	AKKARY ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-21,23 and 24* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-15,17-21,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the RCE filed on 10/19/2006.

2. Claims 11, 12, 17, 18 have been amended.

3. New claims 23 and 24 have been added and examined.

4. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Applicant has provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as US patent 6591342, Akkary et al., at the time this invention was made, or was subject to a joint research agreement at the time this invention was made. However, reference Akkary additionally qualifies as prior art under another subsection of 35 U.S.C. 102, and therefore, is not disqualified as prior art under 35 U.S.C. 103(c).

Applicant may overcome the applied art either by a showing under 37 CFR 1.132 that the invention disclosed therein was derived from the invention of this application, and is therefore, not the invention "by another," or by antedating the applied art under 37 CFR 1.131.

9. Claims 11, 13, 17, 19, and 23-24 rejected under 35 U.S.C. 103(a) as being unpatentable over Akkary et al., US patent 6591342, Martinez et al., "Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors" (hereinafter Martinez), and Gopal, et al., "Speculative Versioning Cache" (hereinafter Gopal).

10. With respect to claims 11 and 17, Akkary teaches of a system comprising: a memory to store at least one store operation (column 1; lines 20-30; the processor

reads the instructions from the software, it is abundantly clear to one of ordinary skill in the art that the instructions must be contained in a memory such as an instruction cache, RAM, or other memory);

a processor to retrieve the at least one store operation from the memory (column 1; lines 20-30, lines 32-34; the processor reads the instructions from the software, and store instructions are a part of the instructions),

the processor including logic to execute the at least one store operation (fig. 8; column 13, lines 1-11; as the processor executes the store operation, it must have logic to do such) and

cause a queue to store a last n stores (fig. 2; column 3, lines 42-60; as a store instruction enters the instruction window, an entry is allocated for it in the store queue. As this is done, there must be logic to do such); and

a circuit to receive and store non-retired stores from said queue (fig. 2, item 230; column 2, lines 45-49; column 4, lines 33-48; SFB is a set-associative buffer that stores store instruction information),

Akkary fails to explicitly teach of wherein said circuit includes at least one storage block to be associated with a checkpoint in a program.

However, Martinez teaches of wherein said circuit includes at least one storage block to be associated with a checkpoint in a program (p. 4, section 2.1; where the backup register file keeps the checkpointed register state).

The combination of Akkary and Martinez fails to explicitly teach of the circuit comprising a speculative data cache.

However, Gopal teaches of a circuit comprising a speculative data cache (fig. 5; p. 5, section 3.2)

Akkary and Martinez are analogous arts as they are both in the same field of endeavor, out-of-order instruction processing. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary and Martinez at the time of the invention to include the checkpoints by the backup register file keeping checkpointed register states in the SFB of Akkary as taught in Martinez. Their motivation would have been to allow the processor to roll back to a prior consistent state if needed (Martinez p. 4; section 2).

The combination of Akkary and Martinez, and Gopal are analogous arts as they are both related to executing load and store operations. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary, Martinez, and Gopal at the time of the invention to make the SFB of the combination of Akkary and Martinez a speculative cache as taught in Gopal. Their motivation would have been to enable a load or store to be speculatively executed before the address of all preceding loads and stores are known (Gopal, abstract).

11. With respect to claims 13 and 19, Akkary fails to explicitly teach of wherein an n-entry buffer stores said queue, and wherein said n-entry buffer is a circular buffer with head and tail pointers.

However, Martinez teaches of wherein an n-entry buffer stores a queue, and wherein said n-entry buffer is a circular buffer with head and tail pointers (p. 2; figure 1).

Akkary and Martinez are analogous arts as they are both in the same field of endeavor, out-of-order instruction processing. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary and Martinez at the time of the invention to include a circular buffer with head and tail pointers in the SQ of Akkary storing the queue as taught in Martinez. Their motivation would have been to reduce the overhead required to maintain the data within the buffer.

12. Claims 14 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Akkary, Martinez, and Gopal as applied to claims 11 and 17 respectively, and further in view of Jourdan, et al., US patent application publication 2003/0217251.

With respect to claims 14 and 20, the combination of Akkary, Martinez, and Gopal fails to explicitly teach of wherein said circuit further comprises a memory dependence predictor to store in a non-tagged array one or more store-distances, wherein said store-distance includes the number of store queue entries between a load and forwarding store.

However, Jourdan teaches of wherein said circuit further comprises a memory dependence predictor to store in a non-tagged array one or more store-distances, wherein said store-distance includes the number of store queue entries between a load and forwarding store (figs. 2, 4; paragraph 0020, 0023, 0024, 0032; as shown in figure 4, the array including the distance entries 400.1-400.k is not tagged).

The combination of Akkary, Martinez, and Gopal, and Jourdan are analogous arts as they are both related to out-of-order instruction processing. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary, Martinez,

Gopal, and Jourdan at the time of the invention to include the dependence predictor in Jourdan into the SFB of the combination of Akkary, Martinez, and Gopal. Their motivation would have been to avoid executing instructions with invalid data and this having re-execute the instructions (Jourdan, paragraph 0002).

13. Claims 12, 15, 18 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Akkary, Martinez, and Gopal as applied to claims 11 and 17 respectively, and further in view of Maier, et al., US patent application publication 2004/0044881.

14. With respect to claims 12 and 18, the combination of Akkary, Martinez, and Gopal fails to explicitly teach of wherein said queue further comprises: an address matching circuit and a store select circuit, wherein both of said address matching circuit and said store select circuit forward stores and/or store data to any dependent loads.

However, Maier teaches of wherein said queue further comprises: an address matching circuit (fig. 1-2; paragraph 0004; where the fields that make up the addresses of the store instructions are compared with that of load instructions. It is abundantly clear to one of ordinary skill in the art that this is done with address match circuitry); and

a store select circuit (fig. 1-2; paragraph 0004; as they are compared, there must be circuitry that selects each individual store instruction),

wherein both of said address matching circuit and said store select circuit forward stores and/or store data to any dependent loads (fig. 1-2; paragraph 0004).

The combination of Akkary, Martinez, and Gopal, and Maier are analogous arts as they are both related to out-of-order instruction processing. It would have been obvious to one of ordinary skill in the art having the teachings of Akkary, Martinez,

Gopal, and Maier at the time of the invention to include the special bypass buffer and process of speculating instruction dependency and forwarding information to the dependent loads into the store queue of the combination of Akkary, Martinez, and Gopal. Their motivation would have been to reduce the complexity of control logic involved (Maier, paragraph 0003).

15. With respect to claims 15 and 21, the combination of Akkary, Martinez, and Gopal fails to explicitly teach of a circuit further comprises an unresolved address buffer to determine a program order condition, wherein said program order condition includes whether one or more non-issued load instructions are scheduled ahead of one or more associated store instructions.

However, Maier teaches of a circuit further comprises an unresolved address buffer to determine a program order condition, wherein said program order condition includes whether one or more non-issued load instructions are scheduled ahead of one or more associated store instructions (paragraph 0004; where in the special bypass buffer, the IDU compares instruction fields used for address generation of load instruction against store instructions. If a match is determined, it is speculated that the load instruction is dependent on the store instruction, and the address field of the store instruction is transferred to the load instruction. It is abundantly clear to one of ordinary skill in the art that this is done to avoid the potential of errors created having the dependent load instruction executing ahead of the store instruction).

The combination of Akkary, Martinez, and Gopal, and Maier are analogous arts as they are both related to out-of-order instruction processing. It would have been

obvious to one of ordinary skill in the art having the teachings of Akkary, Martinez, Gopal, and Maier at the time of the invention to include the special bypass buffer and process of speculating instruction dependency of unresolved instructions into the SFB of the combination of Akkary, Martinez, and Gopal. Their motivation would have been to reduce the complexity of control logic involved (Maier, paragraph 0003).

Response to Arguments

16. Applicant's arguments filed on 10/19/2006 have been fully considered but they are not persuasive.

17. The applicant argues that Akkary is disqualified prior art under 35 USC § 103(c). The examiner would like to point out that Akkary also qualifies as prior art under 35 USC §102(a).

Conclusion

18. This is an RCE of Application No. 10/724,863. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

19. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

PIERRE BATAILLE
PRIMARY EXAMINER
11/13/06